

What is claimed as new and desired to be protected by Letters Patent
of the United States is:

1. A method of fabricating a thin film transistor comprising the
steps of:

providing a gate over a substrate;

providing a gate insulating layer over said gate and said substrate;

providing a silicon layer having a first resistance over said gate
insulating layer;

providing an impurity over said amorphous silicon layer;

forming a drain electrode and a source electrode separated by a
channel region over a contact portion with said amorphous silicon; and

removing said impurity from said channel region and diffusing said
impurity into said contact portion to form a contact layer wherein said contact
layer has a second resistance at least lower than said first resistance.

2. The method of claim 1 wherein said contact layer contains a
concentration of said impurity of at least 0.01%.

09902170.07.1101

5

10

15

amb.
131

3. The method of claim 1 wherein said removing of said impurity from said channel region is performed by exposure to hydrogen plasma.

4. The method of claim 3 wherein said exposure is conducted for about 100 – 130 seconds using a plasma chemical vapor deposition apparatus.

5. The method of claim 1 wherein said diffusion of said impurity into said contact region is performed by heat annealing.

6. The method of claim 5 wherein said heat annealing is conducted at a temperature of about 300⁰C – 320⁰C for about 10 – 15 minutes.

7. The method of claim 1 wherein said impurity is phosphorus.

8. The method of claim 1 wherein said amorphous silicon film is deposited to a thickness of about 150 nm – 200 nm.

9. The method of claim 1 wherein said diffusing step is performed simultaneously with an annealing step for a capping layer provided over said electrodes and said channel region.

10. The method of claim 1 wherein said silicon layer is amorphous.

11. The method of claim 1 wherein said silicon layer is etched utilizing a common photoresist used to form said electrodes.

09902170-071101
Rab.
B2

12. The method of claim 1 wherein said steps are entirely conducted by using an etching apparatus and a protection film forming apparatus while connected in a vacuum state.

13. A method of fabricating a thin film transistor comprising the steps of:

providing a gate over a substrate;

providing a gate insulating layer over said gate and said substrate;

providing a silicon layer having a first resistance over said gate insulating layer;

providing an impurity over said amorphous silicon layer;

etching said silicon layer utilizing a common photoresist used to form a drain electrode and a source electrode separated by a channel region over a contact portion with said amorphous silicon; and

removing said impurity from said channel region and diffusing said impurity into said contact portion to form a contact layer wherein said contact layer has a second resistance at least lower than said first resistance.

09902170.071101

5

Sub.
133

10

15

14. The method of claim 13 wherein said contact layer contains a concentration of said impurity of at least 0.01%.

15. The method of claim 13 wherein said removing of said impurity from said channel region is performed by exposure to hydrogen plasma.

16. The method of claim 15 wherein said exposure is conducted for about 100 – 130 seconds using a plasma chemical vapor deposition apparatus.

17. The method of claim 13 wherein said diffusion of said impurity into said contact region is performed by heat annealing.

18. The method of claim 17 wherein said heat annealing is conducted at a temperature of about 300⁰C – 320⁰C for about 10 – 15 minutes.

19. The method of claim 13 wherein said impurity is phosphorus.

20. The method of claim 13 wherein said amorphous silicon film is deposited to a thickness of about 150 nm – 200 nm.

21. The method of claim 13 wherein said diffusing step is performed simultaneously with an annealing step for a capping layer provided over said electrodes and said channel region.

22. The method of claim 13 wherein said silicon layer is amorphous.

09902170-071101
10002106000

23. The method of claim 13 wherein said steps are entirely conducted by using an etching apparatus and a protection film forming apparatus while connected in a vacuum state.

24. A method of fabricating a thin film transistor comprising the steps of:

providing a gate over a substrate;

providing a gate insulating layer over said gate and said substrate;

providing a silicon layer having a first resistance over said gate insulating layer;

providing an impurity over said amorphous silicon layer;

providing a photoresist over said impurity provided silicon layer and back exposing said photoresist utilizing said gate as a mask and developing a pattern substantially identical with that of said gate;

removing said pattern and forming a drain electrode and a source electrode separated by a channel region over a contact portion with said amorphous silicon; and

09902170.071101

5

10

15

Rev.
134

removing said impurity from said channel region and diffusing said impurity into said contact portion to form a contact layer wherein said contact layer has a second resistance at least lower than said first resistance.

25. The method of claim 24 wherein said contact layer contains a concentration of said impurity of at least 0.01%.

26. The method of claim 24 wherein said removing of said impurity from said channel region is performed by exposure to hydrogen plasma.

27. The method of claim 26 wherein said exposure is conducted for about 100 – 130 seconds using a plasma chemical vapor deposition apparatus.

28. The method of claim 24 wherein said diffusion of said impurity into said contact region is performed by heat annealing.

29. The method of claim 28 wherein said heat annealing is conducted at a temperature of about 300°C – 320°C for about 10 – 15 minutes.

30. The method of claim 24 wherein said impurity is phosphorus.

31. The method of claim 24 wherein said amorphous silicon film is deposited to a thickness of about 150 nm – 200 nm.

0990210-021101

32. The method of claim 24 wherein said diffusing step is performed simultaneously with an annealing step for a capping layer provided over said electrodes and said channel region.

33. The method of claim 24 wherein said silicon layer is amorphous.

34. The method of claim 24 wherein said steps are entirely conducted by using an etching apparatus and a protection film forming apparatus while connected in a vacuum state.

35. A thin film transistor comprising:

a gate provided over a substrate;

a gate insulating layer provided over said gate and said substrate;

a silicon layer having a first resistance provided over said gate insulating layer;

an impurity provided over said amorphous silicon layer;

a drain electrode and a source electrode separated by a channel region formed over a contact portion with said amorphous silicon; and

09902170.071101
T01T/0" 04T20660

wherein said impurity from said channel region is removed and said impurity is diffused into said contact portion to form a contact layer wherein said contact layer has a second resistance at least lower than said first resistance.

36. The transistor of claim 35 wherein said contact layer contains a concentration of said impurity of at least 0.01%.

37. The transistor of claim 35 wherein said impurity is phosphorus.

38. The transistor of claim 35 wherein said amorphous silicon film is deposited to a thickness of about 150 nm – 200 nm.

39. The transistor of claim 35 wherein said silicon layer is amorphous.

40. A thin film transistor comprising:

a gate provided over a substrate;

a gate insulating layer provided over said gate and said substrate;

a silicon layer having a first resistance provided over said gate insulating layer;

an impurity provided over said amorphous silicon layer;

09902170.071101
TOT 20.0720660

wherein said silicon layer is etched utilizing a common photoresist used to form a drain electrode and a source electrode separated by a channel region over a contact portion with said amorphous silicon; and

wherein said impurity from said channel region is removed and said impurity is diffused into said contact portion to form a contact layer wherein said contact layer has a second resistance at least lower than said first resistance.

41. The transistor of claim 40 wherein said contact layer contains a concentration of said impurity of at least 0.01%.

42. The transistor of claim 40 wherein said impurity is phosphorus.

43. The transistor of claim 40 wherein said amorphous silicon film is deposited to a thickness of about 150 nm – 200 nm.

44. The transistor of claim 40 wherein said silicon layer is amorphous.

45. A thin film transistor comprising:

a gate provided over a substrate;

a gate insulating layer provided over said gate and said substrate;

a silicon layer having a first resistance provided over said gate insulating layer;

an impurity provided over said amorphous silicon layer;

5 a drain electrode and a source electrode separated by a channel region formed over a contact portion with said amorphous silicon wherein said channel region is formed by providing a photoresist over said impurity provided silicon layer and back exposing said photoresist utilizing said gate as a mask and developing a pattern substantially identical with that of said gate and removing said pattern; and

10 wherein said impurity from said channel region is removed and said impurity is diffused into said contact portion to form a contact layer wherein said contact layer has a second resistance at least lower than said first resistance.

46. The transistor of claim 45 wherein said contact layer contains a concentration of said impurity of at least 0.01%.

15 47. The transistor of claim 45 wherein said impurity is phosphorus.

48. The transistor of claim 45 wherein said amorphous silicon film is deposited to a thickness of about 150 nm – 200 nm.

09902170.071101

49. The transistor of claim 45 wherein said silicon layer is amorphous.

50. A method of fabricating a liquid crystal display (LCD) comprising the steps of:

providing a plurality of thin film transistors arranged on a LCD substrate in a matrix form, each of said thin film transistors fabricated by the steps of:

providing a gate over a substrate;

providing a gate insulating layer over said gate and said substrate;

providing a silicon layer having a first resistance over said gate insulating layer;

providing an impurity over said amorphous silicon layer;

forming a drain electrode and a source electrode separated by a channel region over a contact portion with said amorphous silicon; and

removing said impurity from said channel region and diffusing said impurity into said contact portion to form a contact layer wherein said contact layer has a second resistance at least lower than said first resistance.

09902170.071101

Pub.
5/35

10

15

51. The method of claim 50 wherein said contact layer contains a concentration of said impurity of at least 0.01%.

52. The method of claim 50 wherein said removing of said impurity from said channel region is performed by exposure to hydrogen plasma.

53. The method of claim 52 wherein said exposure is conducted for about 100 – 130 seconds using a plasma chemical vapor deposition apparatus.

54. The method of claim 50 wherein said diffusion of said impurity into said contact region is performed by heat annealing.

55. The method of claim 54 wherein said heat annealing is conducted at a temperature of about 300⁰C – 320⁰C for about 10 – 15 minutes.

56. The method of claim 50 wherein said impurity is phosphorus.

57. The method of claim 50 wherein said amorphous silicon film is deposited to a thickness of about 150 nm – 200 nm.

58. The method of claim 50 wherein said diffusing step is performed simultaneously with an annealing step for a capping layer provided over said electrodes and said channel region.

59. The method of claim 50 wherein said silicon layer is amorphous.

09902170-071101

60. The method of claim 50 wherein said silicon layer is etched utilizing a common photoresist used to formed said electrodes.

61. The method of claim 50 wherein said steps are entirely conducted by using an etching apparatus and a protection film forming apparatus while connected in a vacuum state.

62. A method of fabricating a liquid crystal display (LCD) comprising the steps of:

providing a plurality of thin film transistors arranged on a LCD substrate in a matrix form, each of said thin film transistors fabricated by the steps of:

providing a gate over a substrate;

providing a gate insulating layer over said gate and said substrate;

providing a silicon layer having a first resistance over said gate insulating layer;

providing an impurity over said amorphous silicon layer;

09902170.071101

pub.
136

etching said silicon layer utilizing a common photoresist used to form a drain electrode and a source electrode separated by a channel region over a contact portion with said amorphous silicon; and

removing said impurity from said channel region and diffusing said impurity into said contact portion to form a contact layer wherein said contact layer has a second resistance at least lower than said first resistance.

63. The method of claim 62 wherein said contact layer contains a concentration of said impurity of at least 0.01%.

64. The method of claim 62 wherein said removing of said impurity from said channel region is performed by exposure to hydrogen plasma.

65. The method of claim 64 wherein said exposure is conducted for about 100 – 130 seconds using a plasma chemical vapor deposition apparatus.

66. The method of claim 62 wherein said diffusion of said impurity into said contact region is performed by heat annealing.

67. The method of claim 66 wherein said heat annealing is conducted at a temperature of about 300°C – 320°C for about 10 – 15 minutes.

68. The method of claim 62 wherein said impurity is phosphorus.

09902170.071101

sub.
136

69. The method of claim 62 wherein said amorphous silicon film is deposited to a thickness of about 150 nm – 200 nm.

70. The method of claim 62 wherein said diffusing step is performed simultaneously with an annealing step for a capping layer provided over said electrodes and said channel region.

71. The method of claim 62 wherein said silicon layer is amorphous.

72. The method of claim 62 wherein said steps are entirely conducted by using an etching apparatus and a protection film forming apparatus while connected in a vacuum state.

10 ~~73. A method of fabricating a liquid crystal display (LCD) comprising the steps of:~~

~~providing a plurality of thin film transistors arranged on a LCD substrate in a matrix form, each of said thin film transistors fabricated by the steps of:~~

~~providing a gate over a substrate;~~

~~providing a gate insulating layer over said gate and said substrate;~~

0902170.071101

sub.
B7

12011070.07101
5 providing a silicon layer having a first resistance over said gate insulating layer;

providing an impurity over said amorphous silicon layer;

providing a photoresist over said impurity provided silicon layer and back exposing said photoresist utilizing said gate as a mask and developing a pattern substantially identical with that of said gate;

removing said pattern and forming a drain electrode and a source electrode separated by a channel region over a contact portion with said amorphous silicon; and

10 removing said impurity from said channel region and diffusing said impurity into said contact portion to form a contact layer wherein said contact layer has a second resistance at least lower than said first resistance.

74. The method of claim 73 wherein said contact layer contains a concentration of said impurity of at least 0.01%.

15 75. The method of claim 73 wherein said removing of said impurity from said channel region is performed by exposure to hydrogen plasma.

76. The method of claim 75 wherein said exposure is conducted for about 100 – 130 seconds using a plasma chemical vapor deposition apparatus.

77. The method of claim 73 wherein said diffusion of said impurity into said contact region is performed by heat annealing.

78. The method of claim 77 wherein said heat annealing is conducted at a temperature of about 300⁰C – 320⁰C for about 10 – 15 minutes.

79. The method of claim 73 wherein said impurity is phosphorus.

80. The method of claim 73 wherein said amorphous silicon film is deposited to a thickness of about 150 nm – 200 nm.

81. The method of claim 73 wherein said diffusing step is performed simultaneously with an annealing step for a capping layer provided over said electrodes and said channel region.

82. The method of claim 73 wherein said silicon layer is amorphous.

83. The method of claim 73 wherein said steps are entirely conducted by using an etching apparatus and a protection film forming apparatus while connected in a vacuum state.

✓84. A liquid crystal display device comprising:

a plurality of thin film transistors provided on a LCD substrate in a matrix form, each of said thin film transistors comprising:

09902170.071101

a gate provided over a substrate;

a gate insulating layer provided over said gate and said substrate;

a silicon layer having a first resistance provided over said gate insulating layer;

5 an impurity provided over said amorphous silicon layer;

a drain electrode and a source electrode separated by a channel region formed over a contact portion with said amorphous silicon; and

wherein said impurity from said channel region is removed and said impurity is diffused into said contact portion to form a contact layer wherein said contact layer has a second resistance at least lower than said first resistance.

85. The device of claim 84 wherein said contact layer contains a concentration of said impurity of at least 0.01%.

86. The device of claim 84 wherein said impurity is phosphorus.

87. The device of claim 84 wherein said amorphous silicon film is deposited to a thickness of about 150 nm – 200 nm.

88. The device of claim 84 wherein said silicon layer is amorphous.

09902170-071101

89. A liquid crystal display device comprising:

a plurality of thin film transistors provided on a LCD substrate in a matrix form, each of said thin film transistors comprising:

a gate provided over a substrate;

a gate insulating layer provided over said gate and said substrate;

a silicon layer having a first resistance provided over said gate insulating layer;

an impurity provided over said amorphous silicon layer;

wherein said silicon layer is etched utilizing a common photoresist used to form a drain electrode and a source electrode separated by a channel region over a contact portion with said amorphous silicon; and

wherein said impurity from said channel region is removed and said impurity is diffused into said contact portion to form a contact layer wherein said contact layer has a second resistance at least lower than said first resistance.

90. The device of claim 89 wherein said contact layer contains a concentration of said impurity of at least 0.01%.

91. The device of claim 89 wherein said impurity is phosphorus.

09902170-071101

92. The device of claim 89 wherein said amorphous silicon film is deposited to a thickness of about 150 nm – 200 nm.

93. The device of claim 89 wherein said silicon layer is amorphous.

/94. A liquid crystal display device comprising:

5 a plurality of thin film transistors provided on a LCD substrate in a matrix form, each of said thin film transistors comprising:

a gate provided over a substrate;

a gate insulating layer provided over said gate and said substrate;

10 a silicon layer having a first resistance provided over said gate insulating layer;

an impurity provided over said amorphous silicon layer;

15 a drain electrode and a source electrode separated by a channel region formed over a contact portion with said amorphous silicon wherein said channel region is formed by providing a photoresist over said impurity provided silicon layer and back exposing said photoresist utilizing said gate as a mask and developing a pattern substantially identical with that of said gate and removing said pattern; and

09902170.071101

wherein said impurity from said channel region is removed and said impurity is diffused into said contact portion to form a contact layer wherein said contact layer has a second resistance at least lower than said first resistance.

95. The device of claim 94 wherein said contact layer contains a concentration of said impurity of at least 0.01%.

96. The device of claim 94 wherein said impurity is phosphorus.

97. The device of claim 94 wherein said amorphous silicon film is deposited to a thickness of about 150 nm – 200 nm.

98. The device of claim 94 wherein said silicon layer is amorphous.

09902170-071101